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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,745	12/29/2004	Shunzou Ohshima	Q85443	9192

23373 7590 10/19/2005

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EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/519,745	Applicant(s) OHSHIMA, SHUNZOU	
	Examiner Dharti H. Patel	Art Unit 2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Objections

1. Claims 1 and 3 recite the limitation "the permissible temperature" in the last paragraph of the claims. There is insufficient antecedent basis for this limitation in the claim. Correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmoock et al., Patent No. 6,624,994, in view of Taki et al., Patent No. 6,474,762. With respect to claim 1, Schmoock et al. teaches a multiple over current protection circuit for regulating current through an analog switch. The protection circuit further comprises a DC power source Vin, a load coupled to Vout, and a semiconductor device 32 arranged between the DC power source and the load; providing a circuit element, a line that is connected to the gate of transistor 32, connected to the semiconductor device 32; switching the semiconductor device so that the load is changed between a driving state and a stopping state; cutting off a conduction of the semiconductor device 32 between the DC power source Vin and the load Vout when a voltage drop across the

semiconductor device exceeds a predetermined reference voltage as disclosed in Fig. 2 and Col. 4, lines 43-51 and Abstract, lines 2-8.

However, Schmoock does not disclose setting a constant of the circuit element so that the reference voltage is not greater than a critical voltage, wherein the critical voltage is a product of an on-resistance of the semiconductor device when its channel temperature is at an upper limit of the permissible temperature, and a minimum current value which causes the channel temperature to reach the upper limit of the permissible temperature by the self-heating due to Joule heat.

Taki et al. teaches that it is known in the art to use a product of the current and voltage through and across the switch to set a threshold or critical voltage, and it is known for the voltage to be selected based on current flow that would cause overheating when the circuit operates in its expected environment. Taki et al. also teaches semiconductor devices Q3, Q4, Q5, Q6 to operate in an active area by causing current to flow through the transistors at all times. Taki et al. further teaches that the voltage 0.5 V is a product of an on-resistance 16.2 ohms of the semiconductor devices Q5 and Q6 and a minimum current value 30mA as disclosed in Col. 10, lines 37-48 and Fig. 9.

Both teachings are related by being semiconductor devices such as transistors. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taki et al., which teaches a critical voltage of the circuit element, into the overcurrent

protection circuit taught by Schmoock because such a combination would logically create a protection (overcurrent/ overvoltage) device capable of a user-adjustable threshold or critical voltage setting.

3. With respect to claim 3, Schmoock et al. teaches a multiple over current protection circuit for regulating current through an analog switch. The protection circuit further comprises a DC power source Vin; a load coupled to Vout; and a semiconductor device 32, arranged between the DC power source and the load, and changes the load between a driving state and a stopping state; a circuit element, a line that is connected to the gate of transistor 32, connected to the semiconductor device 32; a comparator 44, comparing a voltage drop across the semiconductor device 32 with a predetermined reference voltage Vref; and a cut off section, cutting a conduction of the semiconductor device 32 between the DC power source Vin and the load Vout when the voltage drop is greater than the predetermined reference voltage Vref as disclosed in Fig. 2 and Col. 4, lines 43-51 and Abstract, lines 2-8. Claim 3 differs from claim 1 by having a comparator to compare a voltage drop across the semiconductor device with a predetermined reference voltage, so the teachings of Schmoock et al. and Taki et al. would apply to reject claim 3.

4. With respect to claims 2 and 4, it is well known practice to select the smallest on-resistance cited in device specifications that indicate changes in device operation due to either configuration variations or expected operating

temperature changes because a higher value would correspond to more heating than desired and would cause damage to the apparatus.

5. ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
10/17/2005

PHUONG T. VU
PRIMARY EXAMINER